AMENDMENTS TO THE CLAIMS

Please **AMEND** claims 22-29, 33 and 34, as shown below.

Please **ADD** claims 35-37, as shown below.

The following is a complete list of all claims in this application.

1-21. (Cancelled)

22. (Currently Amended) A method for manufacturing a thin film transistor array panel ~~used for a liquid crystal display~~, comprising steps of:

forming a gate line and a gate electrode on a substrate by using a first mask;

forming an insulation layer on the gate line and on the gate electrode;

forming a semiconductor layer on the insulating layer;

forming a data line, a source electrode and a drain electrode on the substrate by using a second mask;

forming a passivation film on the semiconductor layer, the data line, the source electrode and the drain electrode by using a third mask, the passivation film exposing a portion of the drain electrode and a portion of the semiconductor layer;

removing the exposed portion of the semiconductor layer; and

forming a pixel electrode connected to the exposed portion of the drain electrode by using a fourth mask.

23. (Currently Amended) The method of claim 22, wherein the passivation film is formed of an opaque material.

24. (Currently Amended) The method of claim 22, wherein ~~a portion of~~ the passivation film ~~is located on~~ overlaps portions of the gate line and the gate electrode.

25. (Currently Amended) The method of claim 24, wherein the ~~removal of~~ step of removing the exposed portion of the semiconductor layer exposes a portion of the insulating layer, and

the method further comprising~~:~~ a step of removing the exposed portion of the insulating layer.

26. (Currently Amended) The method of claim 25, further comprising~~:~~ a step of forming a connection portion on the insulating layer, the connecting portion overlapping ~~that overlaps~~ a part of the gate line ~~on the insulating layer~~.

27. (Currently Amended) The method of claim 26, wherein the passivation film exposes a part of the connection portion, ~~is exposed outside the passivation film~~ and the connection portion is connected to the pixel electrode.

28. (Currently Amended) A method for manufacturing a thin film transistor array panel ~~used for a liquid crystal display~~, comprising steps of:

depositing a first conductive layer on a substrate;

patterning the first conductive layer by using a first mask to form a gate line and a gate electrode;

depositing an insulating layer on the gate line and on the gate electrode~~,~~;

depositing a semiconductor layer on the insulating layer;

depositing a second conductive layer on the insulating layer;

patterning the second conductive layer by using a second mask to form a data line, a source electrode, and a drain electrode;

depositing a passivation layer on the semiconductor layer, the drain electrode, the source electrode and the data line;

patterning the passivation layer by using a third mask to expose a portion of the semiconductor layer, a portion of the gate line, a portion of the data line, a portion of the insulating layer;

removing the exposed portion of the insulating layer;

depositing a third conductive layer on the passivation layer and the insulating layer; and

patterning the third conductive layer to form ~~forming~~ a pixel electrode that contacts the exposed portion of the drain electrode by using a fourth mask.

29. (Currently Amended) The method of claim 28, further comprising~~:~~ a step of forming transparent conductive pads that cover the exposed portion of the gate line and the data line, respectively.

30. (Previously Presented) The method of claim 28, wherein the first conductive layer comprises an upper layer and a lower layer of different materials.

31. (Previously Presented) The method of claim 30, wherein the lower layer comprises Al or an Al alloy, and the upper layer comprises Mo.

32. (Previously Presented) The method of claim 30, wherein the lower layer comprises Cr, and the upper layer comprises Al or an Al alloy.

33. (Currently Amended) The method of claim 32, further comprising: a step of removing the exposed portion of the upper layer.

34. (Currently Amended) The method of claim ~~33~~ 28, wherein the step of depositing a semiconductor layer comprises steps of:

depositing an amorphous silicon layer on the insulating layer; and

depositing a n+ amorphous silicon layer on the amorphous silicon layer ~~wherein the patterning of the second conductive layer exposes a portion of the n+ amorphous silicon layer, and further comprising:~~

~~removing the exposed portion of the n+ amorphous silicon layer after patterning then second conductive layer~~.

35. (New) The method of claim 34, wherein the step of patterning the second conductive layer exposes a portion of the n+ amorphous silicon layer.

36. (New) The method of claim 35, further comprising a step of removing the exposed portion of the n+ amorphous silicon layer.

37. (New) The method of claim 36, wherein the step of removing the exposed portion of the n+ amorphous silicon layer exposes a portion of the amorphous silicon layer.